ABSTRACT

Methods and apparatuses associated with an L0 instruction cache. An L0 instruction cache stores sequences of instruction data and can be accessed in a single instruction clock cycle. In one embodiment pointers are used to define a window of valid instruction data. Instructions are stored in the cache sequentially, without empty memory space between the end of one instruction and the beginning of another. Instructions are read and aligned from the L0 cache and sent to the instruction latch. Alignment is performed with a permutation unit that correctly orders the separate instruction data elements read from the cache memory.